CLAIMS
What is claimed is:

1. A method comprising:

receiving a first data signal generated with respect to a first clock signal associated with a first time domain;

receiving a second data signal representing said first data signal delayed by a first measure such that during transition of said first data signal said second data signal is valid, and during transition of said second data signal said first data signal is valid;

receiving a selector signal to select one of said first and second data signals, said selector signal representing said first clock signal delayed by a second measure such that at any given sampling point of said selector signal said selector signal will select valid data;

receiving a second clock signal associated with a second time domain; and

sampling said selector signal and said first and said first and second data signals based upon said second clock signal to output the selected one of said first and second data signals with respect to said second time domain.

2. The method of claim 1, wherein said second measure is half of said first measure.

3. The method of claim 2, wherein said second data signal is delayed an amount sufficient to cause said second data signal to be approximately 180

degrees out of phase with respect to said first data signal and said third signal is delayed an amount sufficient to cause said third signal to be approximately 90 degrees out of phase with respect to said reference signal.

4. The method of claim 1, wherein said first time domain is asynchronous to said second time domain.

5. The method of claim 1, wherein said selector signal alternatingly selects between said first and second data signals.

6. The method of claim 5, wherein said selector signal is in a first signal state while said first data signal is valid and said selector signal is in a second signal state while said second data signal is valid.

7. The method of claim 5, wherein said second clock signal has a frequency that is approximately double that of the first clock signal.

8. The method of claim 1, wherein said data signal is generated by a multi-bit data bus.

9. A method of passing data between a first time domain and a second asynchronous time domain, the method comprising:

receiving a first data signal generated with respect to a reference signal associated with said first time domain, said reference signal having a period of N;

receiving a second data signal, said second data signal being phase-shifted by a factor of N/2 with respect to said first data signal;

receiving a third signal, said third data signal being phase-shifted by a factor of N/4 with respect to said reference signal;

sampling said first data signal, said second data signal and said third signal based upon a clock signal of said second time domain; and

selecting one of said first and second data signals based at least in part upon said third signal to output valid data independent of said first and second data signal states at the time of sampling.

10. The method of claim 9, wherein said second signal is approximately 180 degrees out of phase with respect to said first data signal and said third data signal is approximately 90 degrees out of phase with respect to said reference signal.

11. The method of claim 9, wherein said data signal is generated by a multi-bit data bus.

12. A method of passing data between a first time domain and a second asynchronous time domain, the method comprising:

receiving a first data signal generated with respect to a first clock signal associated with said first time domain;

receiving a second data signal representing said first data signal delayed by a first measure such that during transition of said first data signal said second data signal is valid, and during transition of said second data signal said first data signal is valid; and

selecting between said first and second data signals based at least in part upon the state of a second clock signal associated with said second time domain.

13. The method of claim 12, further comprising:

receiving a selector signal to select one of said first and second data signals, said selector signal representing said first clock signal delayed by a second measure such that at any given sampling point of said selector signal said selector signal will select valid data.

14. The method of claim 13, wherein said selecting comprises sampling said selector signal based upon the value of said second clock signal to output the selected one of said first and second data signals.

15. The method of claim 13, wherein said second data signal is delayed an amount of time sufficient to cause said second data signal to be approximately 180 degrees out of phase with respect to said first data signal and said selector

signal is delayed an amount of time sufficient to cause said selector signal to be approximately 90 degrees out of phase with respect to said first clock signal.

16. The method of claim 12, wherein said data signal is generated by a multi-bit data bus.

17. A method comprising:

receiving a first data signal generated with respect to a first clock signal associated with a first time domain;

generating a second data signal based at least in part upon said first data signal, said second data signal being out of phase with respect to said first data signal by a first measure such that during transition of said first data signal said second data signal is valid, and during transition of said second data signal said first data signal is valid;

generating a selector signal such that at any given sampling point of said selector signal said selector signal will indicate a valid one of said first and second data signals;

receiving a second clock signal associated with a second time domain;

and

sampling said selector signal and said first and said first and second data signals based upon said second clock signal to output a selected one of said first and second data signals with respect to said second time domain.

18. The method of claim 17, wherein generating said selector signal comprises a delayed version of said first clock signal.

19. The method of claim 18, wherein said second data signal is approximately 180 degrees out of phase with respect to said first data signal and said selector signal is delayed an amount sufficient to cause said third signal to be approximately 90 degrees out of phase with respect to said first clock signal.

20. An integrated circuit comprising:

a first delay circuit to generate a selector signal based upon an input reference signal of a first time domain;

a second delay circuit to generate a delayed data signal based upon an input data signal; and

selection logic coupled to the first and second delay circuits to select one of said data signal and said delayed data signal based upon the state of the selector signal in accordance with an input clock signal of a second time domain, such that at any given sampling point of the input clock signal, the selector signal indicates valid data.

21. The apparatus of claim 20, wherein the first delay circuit causes the selector signal to be approximately ninety degrees out of phase with the input reference signal.

22. The apparatus of claim 21, wherein the second delay circuit causes the delayed data signal to be approximately 180 degrees out of phase with the input data signal.

23. The apparatus of claim 20, wherein the selection logic further comprises:

at least two edge triggered flip-flops to latch the data signal and the delayed data signal based upon the input clock signal; and

a multiplexer to select between one of said data signal and said delayed data signal based upon the state of the selector signal.

24. An apparatus comprising:

first logic to:

receive a first data signal generated with respect to a first clock signal associated with said first time domain,

receive a second data signal representing said first data signal delayed by a first measure such that during transition of said first data signal said second data signal is valid, and during transition of said second data signal said first data signal is valid; and

receive a selector signal representing said first clock signal delayed by a second measure such that at any given sampling point of said selector signal said selector signal will indicate valid data, and

receive a second clock signal associated with said second time domain to sample said first data signal, said second data signal, and said selector signal; and

second logic coupled to said first logic to select between said first and second data signals based upon the sampled value of said selector signal.

25. The apparatus of claim 24, further comprising:

a first delay circuit to generate said second data signal based at least in part upon said first data signal; and

a second delay circuit to generate said selector signal based at least in part upon said first clock signal.

26. The apparatus of claim 25, wherein said first delay circuit delays said first data signal such that said second data signal is approximately 180 degrees out of phase measure with respect to said first data signal.

27. The apparatus of claim 25, wherein said delay second delay circuit delays said first clock signal such that said selector signal is approximately 90 degrees out of phase measure with respect to said first clock signal.